Hall Ticket Number:

Code No. : 22666

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

M.E. (E.C.E.) II-Semester Main Examinations, August-2023

CPLD & FPGA Architectures and Applications (PE-III)

(Embedded Systems & VLSI Design)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Find the number of address lines and number of output lines does the 1024 × 8 PROM device support.	2	2	1	3
2.	The size of a PLA device is specified with 3×8×4. What does each dimension specifies?	2	1	1	3
3.	Draw the architecture block diagram of a PAL device.	2	1	2	3
4.	List the Simple Programmable Logic Devices (SPLDs).	2	1	2	3
5.	Distinguish between PAL and PLA devices.	2	2	2	3
6.	List the applications of Programmable Logic Devices (PLDs)	2	1	2	3
7.	Find the number of 2×1 Muxes required to realize 2-input LUT.	2	2	3	4
8.	Find the number of 4-input LUTs required to realize 7-input LUT. Also find the number of 2×1 Muxes required.	2	2	3	4
9.	Distinguish between EPROM and EEPROM.	2	2	4	3
10.	What is the function of product term allocator in CPLD architecture?	2	1	4	3
	Part-B (5 × 8 = 40 Marks)				
11. a)	The following logic functions are to be implemented using a PLA device. $F_0 = A\bar{C} + AB, F_1 = A + \bar{B}\bar{C}$, $F_2 = \bar{B}\bar{C} + AB, F_3 = \bar{B}C + A$ Calculate the hardware cost in terms of number of inverters, buffers, AND gates and OR gates required.	4	3	1	1
b)	Realize the hardware logic diagram to implement the following functions using PAL device. $F_1 = x_1\, x_2\, x_3' + x_1'\, x_2\, x_3$ $F_2 = x_1'\, x_2' + x_1\, x_2\, x_3$	4	4	1	1

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12. a)	Construct and draw the logic diagram for 32×4 PROM device.	4	1	2	3
b)	Analyze and compare the key characteristics of PROM device with reference to PLA and PAL devices.	4	3	2	3
13. a)	Design the following function generator using PROM device. $F(x) = x^2$ where x is a 3 bit unsigned binary number.	4	3	3	3
b)	Derive the PLA programming table to realize the following Boolean expressions. $F_1(A,B,C) = (0,1,3,4), \quad F_2(A,B,C) = (1,2,3,4,5)$	4	4	3	3
14. a)	Design a full adder using a PROM device.	4	3	2	1
b)	Analyse and bring out the differences between the processor and FPGA.	4	3	5	1
15. a)	2×1 Mux is the basic building block to realize LUT. Draw the block diagram of 2×1 Mux and also draw the logic circuit diagram of 2×1 Mux	4	3	5	4
b)	Analyze and find the number of 4 input LUTs required to realize full adder.	4	2	5	4
16. a)	Which of the following functional descriptions can be realized by a single 4-input LUT in a typical FPGA? Justify your answer. (a) F = A'.B.C + B'.C' (b) F = (A.B + A'.B') . (C.D' + C'.D) (c) F = A.B.C + B'.D.E	4	4	5	4
b)	Implement a full adder circuit using 4:1 multiplexers.	4	3	5	4
17.	Answer any ***two*** of the following:				
a)	Realize 3-input LUT using 2-input LUTs and draw its logic diagram.	4	3	3	4
b)	Draw the logic diagram of functional block architecture in CPLD.	4	4	4	3
c)	Implement the following Boolean function in FPGA. $f(A,B,C,D) = \Sigma m(3,5,6,9,10,12)$	4	3	5	4

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	30%
iii)	Blooms Taxonomy Level – 3 & 4	50%

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